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L1 same tester	24

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L29	L1 same tester	24	L29
L28	L27 same (pin or terminal)	15	L28
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L25	l10 same convert$	14992	L25
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L23	smaller near3 number	70480	L23
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L18	L17 and l14	0	L18
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L16	tester same gigibit	0	L16

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L13	L12 same state	43	L13
L12	L11 same (circuit or uut or dut or cut)	113	L12
L11	L10 same l1	135	L11
L10	L9 same connection	178127	L10
L9	switching or matrix	1554338	L9
L8	L1 same test same interface	5	L8
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L4	L3 same l2 same l1	8	L4
L3	common same state	342891	L3
L2	test same circuit	179884	L2
L1	grouping same (input or output) same (pin or terminal)	1365	L1

END OF SEARCH HISTORY

L29: Entry 21 of 24 File: DWPI Dec 8, 1998

DERWENT-ACC-NO: 1999-091043
DERWENT-WEEK: 199908

TITLE: Test pattern production method for LSI inspection - involves generating patterns by providing attributes and grouping of input terminals of tester

PATENT-ASSIGNEE:

ASSIGNEE	CODE
NEC CORP	NIDE

PRIORITY-DATA: 1997JP-0150062 (May 23, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10325856 A	December 8, 1998		011	G01R031/3183

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
JP 10325856A	May 23, 1997	1997JP-0150062	

INT-CL (IPC): G01 R 31/3183; G06 F 11/22

ABSTRACTED-PUB-NO: JP 10325856A
BASIC-ABSTRACT:

The method involves providing attributes to input terminals and grouping of input terminals of a tester. The tester consists of logic circuits such as sequential circuit (10) and combinational circuit (16). An excellent article discrimination test is performed on the tester in order to verify whether there is any fault in the output of the tester, which is caused by skew between input and output terminals.

A pattern is applied to the input terminals of the tester during discrimination test. The input terminals are then grouped, thereby reducing amount of delay, introduced by the patterns between the grouped terminals.

ADVANTAGE - Reduces amount of patterns inserted to tester. Reduces delay between patterns applied to grouped input terminals.

CHOSEN-DRAWING: Dwg.1/12

TITLE-TERMS: TEST PATTERN PRODUCE METHOD LSI INSPECT GENERATE PATTERN ATTRIBUTE

GROUP INPUT TERMINAL TEST

DERWENT-CLASS: S01 T01

EPI-CODES: S01-G01; T01-G02A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1999-066992

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L29: Entry 20 of 24 File: DWPI Jul 4, 2000

DERWENT-ACC-NO: 2000-494434
DERWENT-WEEK: 200222

TITLE: Test group formation apparatus for testing large scale integrated circuit, has output unit to output grouping information produced by group production in desired format according to grouping conditions

PATENT-ASSIGNEE:

ASSIGNEE	CODE
NEC CORP	NIDE

PRIORITY-DATA: 1998JP-0365449 (December 22, 1998)

PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	JP 2000187064 A	July 4, 2000		007	G01R031/3183
☐	JP 3267258 B2	March 18, 2002		005	G01R031/3183

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
JP2000187064A	December 22, 1998	1998JP-0365449	
JP 3267258B2	December 22, 1998	1998JP-0365449	
JP 3267258B2		JP2000187064	Previous Publ.

INT-CL (IPC): G01 R 31/28; G01 R 31/3183; G06 F 11/22; G06 F 17/50

ABSTRACTED-PUB-NO: JP2000187064A
BASIC-ABSTRACT:

NOVELTY - A logic pin tester pin correspondence unit (31) supplies information to a LSI pin component (4) and tester pin of LSI pin (1). A group production unit (32) produces a group of thin component information according to grouping conditions (2) which guide division of test group. An output unit (33) outputs the grouping information in desired format.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for test group formation method.

USE - For manufacturing test group used for testing large scale integrated circuit.

ADVANTAGE - Even when a complicated IC has large number of pins, grouping of pins

can be performed automatically in short time.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of test group manufacturing apparatus.

LSI pin 1

Grouping condition 2

LSI pin component 4

Logic pin tester pin correspondence unit 31

Group production unit 32

Output unit 33

CHOSEN-DRAWING: Dwg.1/6

TITLE-TERMS: TEST GROUP FORMATION APPARATUS TEST SCALE INTEGRATE CIRCUIT OUTPUT UNIT OUTPUT GROUP INFORMATION PRODUCE GROUP PRODUCE FORMAT ACCORD GROUP CONDITION

DERWENT-CLASS: S01 T01

EPI-CODES: S01-G01A1; T01-G02A1;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2000-367241

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L29: Entry 12 of 24 File: JPAB Jul 4, 2000

PUB-NO: JP02000187064A
DOCUMENT-IDENTIFIER: JP 2000187064 A
TITLE: TEST GROUP FORMING DEVICE AND ITS FORMING METHOD

PUBN-DATE: July 4, 2000

INVENTOR-INFORMATION:
NAME COUNTRY
KONNO, YOSHINOBU

ASSIGNEE-INFORMATION:
NAME COUNTRY
NEC CORP

APPL-NO: JP10365449
APPL-DATE: December 22, 1998

INT-CL (IPC): G01 R 31/3183; G01 R 31/28; G06 F 11/22; G06 F 17/50

ABSTRACT:

PROBLEM TO BE SOLVED: To form test groups without failure and in a short time in spite of complication in a semiconductor integrated circuit and increase in the number of pins.

SOLUTION: This device 3 forms test groups of semiconductor integrated circuits LSI. A logic pin-tester pin corresponding means 31 forms a logic pin from LSI pin assign information 1 and, LSI pin constitution information 4 from tester pin information, groups the LSI pin constitution information 4 with a group formation means 32 according to grouping conditions 2, processes the grouped pin information in a format readable with an LSI tester and outputs it from a grouping information output means 33. By defining the grouping conditions in advance, grouping information processed in a readable format in the grouping information output means 33 are output. Even in the case the LSI is complex and the number of pins is increasing, the grouping of pins different for each LSI is automatically made and a test group can be formed in a short time without mistakes.

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L29: Entry 11 of 24 File: USPT Oct 13, 1992

DOCUMENT-IDENTIFIER: US 5155440 A
** See image for Certificate of Correction **
TITLE: Hand-held cable tester

Detailed Description Text (17):
FIGS. 3A and 3B are schematic diagrams of the status display portion of the tester. The display area is configured to accommodate a sixty-pin ribbon cable. This portion of the circuitry is used to display test results during all forms of cable harness evaluation, as well as during self-testing. Beginning at the left side of the diagram, sixty individual outputs 110 of the CMOS comparator bank (80 and 90 in FIG. 1) are fed to eight identical circuit groupings. These circuit groupings develop the error display for the individual wires and are identified as GROUP X (where X represents the group number). With the exception of GROUP 8, all groups in this configuration accommodate eight comparator outputs. Because the tester is preset to handle a sixty-pin cable harness, GROUP 8 receives only four comparator outputs. Within each group, every comparator output is connected to a programmable DIP switch 120. Assuming that each of these switches is closed, each comparator output is connected to two components:

L29: Entry 10 of 24 File: USPT Jul 6, 1993

DOCUMENT-IDENTIFIER: US 5226048 A
TITLE: At-speed testing of core logic

Detailed Description Text (28):
Advantageously, inputs and outputs having the same timing relationships can be grouped together for purposes of the at-speed testing technique of this invention. Such grouping will make the characterization, and analysis of its results, manageable. The input pins which are defined to be in the same group can share the same timing generators for splots. The output pins that are grouped together can be tested against the same tester strobe setting. If any of the outputs in a specific group fails to meet the limits, the splot will show a failure. Full characterization, where all the input and output delays and the timing relationships are individually measured is not recommended. The completion time would be very long and costly.

L29: Entry 4 of 24 File: USPT Jun 18, 2002

DOCUMENT-IDENTIFIER: US 6407572 B1
TITLE: System and method for testing and evaluating a device

Detailed Description Text (12):
Further, the system 10 for testing and evaluating the LSI device shown in FIG. 2 comprises a unit 50 for obtaining and storing information related to various testing conditions of the LSI device and sending out the same information to the system controller 6. The testing conditions for the LSI device include the source voltage supplied to the LSI device, an input level for applying an input, an output level for determining an output and the signal timing. The information for setting these testing conditions is digitized when reading the testing conditions from the body of the LSI tester 7. Further, the system 10 for testing and evaluating the LSI device comprises a unit 20 for classifying pins into a plurality pin types and storing the pin types by grouping the pins into a plurality of pin types having the same testing condition data, based on the information of each pin for setting the testing conditions of the LSI device. The pin data classified into a plurality of pin types is stored in the RAM or the like of the unit 20.

L29: Entry 3 of 24 File: USPT Jul 1, 2003

DOCUMENT-IDENTIFIER: US 6587976 B1
TITLE: Semiconductor device tester for measuring skew between output pins of a semiconductor device

Detailed Description Text (11):
A further embodiment of the present invention will now be described with reference to the schematic block diagram of FIG. 4 and the timing diagrams of FIGS. 5a-5d. As shown in FIG. 4, a tester 400 is interfaced to a plurality of input/output pins of the semiconductor device 100. The illustrated tester 400 includes various circuits previously described with reference to the tester 200 shown in FIG. 1 which will not be further described herein. In addition, the tester 400 includes a plurality of comparator circuits coupled to the plurality of output pins of the semiconductor device 100 that generate a skew signal having a duration corresponding to a time period when data on respective ones (three in each grouping in the embodiment of FIG. 4) of the output pins differs. The comparator circuits include exclusive OR (XOR) gates 42-1, 42-2, . . . , 42-(n/3), exclusive NOR (XNOR) gates 44-1, 44-2, . . . , 44-(n/3) (also referred to as equivalence AND gates), each of which inputs three output data signals from three of the input/output pins of the semiconductor device 100, and SR flip flops 40-1, 40-2, . . . , 40-(n/3). SR flip flops 40-1, 40-2, . . . , 40-(n/3) have S (set) inputs coupled to the outputs of associated ones of the XOR gates 42-1, 42-2, . . . , 42(n/3) and R (reset) inputs coupled to the outputs of associated ones of the XNOR gates 44-1, 44-2, . . . , 44-(n/3). Accordingly, the comparator circuits respectively provide for measurement of skews between data output from their associated three data input/output pins of the semiconductor device 100

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L29: Entry 1 of 24 File: USPT Sep 21, 2004

DOCUMENT-IDENTIFIER: US 6794861 B2
TITLE: Method and apparatus for socket calibration of integrated circuit testers

Detailed Description Text (18):
A source synchronous bus is a set of input or output conductors (in this case on an integrated circuit) in which the timing is specified only with respect to an input or an output clock signal that is associated with the bus. ("Bus" generally refers to a grouping of channels carrying I/O signals here.) In this case a bus is a group or bundle of channels each associated with an input/output terminal where the bus has an associated clock signal. The timing relationships to all the other pins of the device under test are specified much more loosely (or not at all). This has been found to dramatically reduce the number of reference blocks required in order to calibrate the tester for testing the entire DUT.

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L4: Entry 1 of 8 File: TDBD Dec 1, 1978

DOCUMENT-IDENTIFIER: NN78122785
TITLE: Method for Simultaneous Generation of Multiple Tests for LSSD Logic Circuits. December 1978.

Disclosure Text (1):
2p. Single latch designs with the LSSD (level sensitive scan design) discipline have the general structure depicted in the drawing. For further information on LSSD, see U. S. Patent 3,783,254. - In the configuration shown, only one of the two clocks (C1 and C2) can be turned on at one time, otherwise, race conditions will occur. Frequently, large amounts of logic having single latch designs end up with many groups of clocks such that only the clocks within one group may be turned on simultaneously without causing races. Such groups are referred to as clock groups. Furthermore, LSSD-type tests ("combinational tests") have a structure in which the clocked-in value of a latch can depend only on the values on the external input pins or on the scanned-in states of the various SRLs (shift register latches). Hence, an LSSD test can only turn on clocks that are in the same clock group (in addition to the B clocks). Traditionally, the deterministic test pattern generators recognize this constraint and generate LSSD tests only. - Consider the circuit in the drawing. An LSSD test will allow detection of faults either from the logic X or from the logic Y but not from both (since only one of C1/C2 can be turned on). Let us assume (for the sake of explanation) that C1 is turned on in an LSSD test. In this case, all implications (equivalent to 3 value zero delay simulation) of logic assignments to the X set of L1 latches are propagated into the X logic and are wasted. This waste will be avoided in the disclosed method. When coupled with the concept of dynamic subsumation *ù (allows detection of several faults using a common set of assignments to PIs/SRLs), the realized savings are further increased. Making the idealized assumptions that equal amounts of exclusive combinational logic are associated with each clock group (e.g., X logic is associated with clock C2 and Y logic is associated with clock C1), there is a waste of n-1 over n of the implication costs for n clock groups. It is this waste that is proposed to be recovered under the disclosed method. Proposed Method 1. For each clock Ci, determine a race list of all the clocks Ci1, Ci2, ---- which cannot be turned on without causing a race condition. 2. Generate a set of assignments (on PIs (primary inputs) and SRLs) to detect several faults (using dynamic subsumation) while ignoring the constraint imposed by the clock grouping. 3. The number of tester loops generated from each set of assignments (on PIs/SRLs) is equal to the number of race-free clock groups into which the "on" clocks (clock PI at "on" state) may be divided. Each tester loop consists of identical assignments to the SRLs and the nonclock PIs. The clock PIs that are "off" remain as such in each tester loop. The "on" clock PIs are analyzed for clock grouping to create the difference between the tester loops. In fact, the tester loops produced from a set of PI/SRL assignments are such that i) an "on" system clock is pulsed in, at most, one of the tester loops, and ii) the tester loops differ only in the system clocks that are pulsed in the tester loop. Process for Determining Race-free Clock Groups in Step 3 a) Initialize all "on" clock PIs to be unused and enabled. b) If no unused "on" clocks, then DONE. c) Find next unused, enabled "on" clock PI. If none found, then go to step f. d) Set the disabled flag on all the as yet unused and enabled "on" clock PIs that are in the race list for the clock found in the last execution of step c. e) Return to step c. f) Issue a tester loop containing a pulse each on those clock PIs which were found in step c of this iteration i. g) Set the "used"

flag on all clocks pulsed in the tester loop generated in step f. h) Remove the disabled flag from all clocks, and go to step b. Reference *ù P. Goel, "Dynamic Subsumation of Test Patterns for LSSD Systems," IBM Technical Disclosure Bulletin 21, 2782-2784 (December 1978, this issue).

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L4: Entry 1 of 8 File: TDBD Dec 1, 1978

TDB-ACC-NO: NN78122785

DISCLOSURE TITLE: Method for Simultaneous Generation of Multiple Tests for LSSD Logic Circuits. December 1978.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, December 1978, US

VOLUME NUMBER: 21
ISSUE NUMBER: 7
PAGE NUMBER: 2785 - 2786

PUBLICATION-DATE: December 1, 1978 (19781201)

CROSS REFERENCE: 0018-8689-21-7-2785

DISCLOSURE TEXT:

2p. Single latch designs with the LSSD (level sensitive scan design) discipline have the general structure depicted in the drawing. For further information on LSSD, see U. S. Patent 3,783,254. - In the configuration shown, only one of the two clocks (C1 and C2) can be turned on at one time, otherwise, race conditions will occur. Frequently, large amounts of logic having single latch designs end up with many groups of clocks such that only the clocks within one group may be turned on simultaneously without causing races. Such groups are referred to as clock groups. Furthermore, LSSD-type tests ("combinational tests") have a structure in which the clocked-in value of a latch can depend only on the values on the external input pins or on the scanned-in states of the various SRLs (shift register latches). Hence, an LSSD test can only turn on clocks that are in the same clock group (in addition to the B clocks). Traditionally, the deterministic test pattern generators recognize this constraint and generate LSSD tests only. - Consider the circuit in the drawing. An LSSD test will allow detection of faults either from the logic X or from the logic Y but not from both (since only one of C1/C2 can be turned on). Let us assume (for the sake of explanation) that C1 is turned on in an LSSD test. In this case, all implications (equivalent to 3 value zero delay simulation) of logic assignments to the X set of L1 latches are propagated into the X logic and are wasted. This waste will be avoided in the disclosed method. When coupled with the concept of dynamic subsumation *ù (allows detection of several faults using a common set of assignments to PIs/SRLs), the realized savings are further increased. Making the idealized assumptions that equal amounts of exclusive combinational logic are associated with each clock group (e.g., X logic is associated with clock C2 and Y logic is associated with clock C1), there is a waste of n-1 over n of the implication costs for n clock groups. It is this waste that is proposed to be recovered under the disclosed method. Proposed Method 1. For each clock Ci, determine a race list of all the clocks Ci1, Ci2, ---- which cannot be turned on without causing a race condition. 2. Generate a set of assignments (on PIs (primary inputs) and SRLs) to detect several faults (using dynamic subsumation) while ignoring the constraint imposed by the clock grouping. 3. The number of tester loops generated from each set of assignments (on PIs/SRLs) is equal to the number of race-free clock groups into which the "on" clocks (clock PI at "on" state) may be divided. Each tester loop consists of identical assignments to the SRLs and the

nonclock PIs. The clock PIs that are "off" remain as such in each tester loop. The "on" clock PIs are analyzed for clock grouping to create the difference between the tester loops. In fact, the tester loops produced from a set of PI/SRL assignments are such that i) an "on" system clock is pulsed in, at most, one of the tester loops, and ii) the tester loops differ only in the system clocks that are pulsed in the tester loop. Process for Determining Race-free Clock Groups in Step 3 a) Initialize all "on" clock PIs to be unused and enabled. b) If no unused "on" clocks, then DONE. c) Find next unused, enabled "on" clock PI. If none found, then go to step f. d) Set the disabled flag on all the as yet unused and enabled "on" clock PIs that are in the race list for the clock found in the last execution of step c. e) Return to step c. f) Issue a tester loop containing a pulse each on those clock PIs which were found in step c of this iteration i. g) Set the "used" flag on all clocks pulsed in the tester loop generated in step f. h) Remove the disabled flag from all clocks, and go to step b. Reference *ù P. Goel, "Dynamic Subsumation of Test Patterns for LSSD Systems," IBM Technical Disclosure Bulletin 21, 2782-2784 (December 1978, this issue).

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L8: Entry 2 of 5 File: USPT Jun 9, 1998

DOCUMENT-IDENTIFIER: US 5764069 A
TITLE: High density grid for testing circuit boards

Abstract Text (1):
A test interface between an electrical circuit to be tested and a test controller generally includes a plurality of translation pins, a plurality of grid boards and a connector to a controller. Each translation pin has a first end disposed for electrical contact with a point to be tested on the circuit to be tested and has a second end; the second ends collectively forming an output grid. Each grid board includes a plurality of grid contacts printed on a peripheral receiving edge perpendicular to the boards faces. The plurality of grid boards are disposed such that the grid contacts form a receiving grid congruent with the output grid such that individual ones of the second ends of the translation pins make electrical contact with individual ones of the grid contacts. In an exemplary embodiment, the grid boards are arranged in groupings, each grouping including a switching grid board, at least one receiving grid board and electrical connection between the buss contacts of the receiving grid board and a circuit on the switching grid board. According to another embodiment of the invention, the high-density interface is integrated into a low-density interface by disposition between the low-density output grid and the electrical circuit to be tested.

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